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RYAN, MASON & LEWIS, LLP
1300 POST ROAD
SUITE 205
FAIRFIELD, CT 06824

EXAMINER	
HIDALGO, FERNANDO N	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/586,176	KOHLER ET AL.	
	Examiner	Art Unit	
	FERNANDO N. HIDALGO	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 July 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/18/07, 7/17/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. **Claim(s) 1-5, 11-15, 21 and 23-30** are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Publication No. 2005/0146932 A1 to Lee et al. ("Lee").

As to **claim 1**, Lee discloses a method (the method inherently taught by the device) for programming a one time programmable memory (Page 4, paragraph [0052] discloses a proposed extended OTP, one time programmable, memory cell), wherein the improvement comprises the steps of: obtaining an array of transistors (FIG. 4 shows an array of memory cell transistors 402, 404 and the like); and programming at least one of said transistors using a hot carrier transistor aging technique to alter a characteristic of said at least one of said transistor (FIG. 6, page 3, paragraph [0040] disclose an OTP cell programmed by hot-electron (hot carrier) wherein, a high positive voltage applied to the source or drain accelerates electron carriers through the transistor channel and at the same time a high positive voltage applied to the gate of the transistor pulls the carriers to the transistor thin oxide).

As to **claim 2**, Lee discloses that said programming step further comprises the step of applying a stressful voltage to said at least one of said transistors to cause said hot carrier transistor aging (FIG. 6 shows a memory cell of an array (FIG. 4) wherein, a stressful high voltage is applied to the transistor cell, the stressful voltage is disclosed to have a typical value of 37 Volts, page 3, paragraph [0040]).

As to **claim 3**, Lee discloses that said altered characteristic is a change in a threshold voltage of said at least one of said transistors (page 3, paragraph [0042] disclose that after programming, the charge stored is removed and “threshold voltage of memory cell descends from program cell Vt;" that is, the initial non-programmed cell has achieved a threshold voltage value after programming).

As to **claim 4**, Lee discloses that said programming step further comprising the step of applying a stressful voltage to a drain and a gate of said at least one of said transistors to cause said change in said threshold voltage of said at least one of said transistors (FIG. 6 shows steps of voltage stressing the gate with VPP1 voltage level, and voltage stressing the source/drain (MOS transistors are inherently symmetrical with respect to the drain and source terminals, and such terminals S/D or D/S are inherently interchangeable; further, claim 1 of Lee reinforces this position by, for example, referring to a "first source/drain (S/D) region and a second S/D region") with VPP1 voltage level).

As to **claim 5**, Lee discloses detecting said programmed at least one of said transistors by sensing said change in said threshold voltage of said at least one of said transistors (**(Note: detecting defined as sensing by a read operation, after programming, of a memory cell in the specifications on page 4, last paragraph).** Page 3, paragraph [0043] disclose a reading operation for sensing the programmed threshold voltage; that , as disclosed in Table 1, the transistor memory is biased differently from that of programming so as to not to disturb the programming threshold voltage, thus sensing and unchanging the threshold voltage as set by programming).

As to **claim 11**, Lee discloses a one time programmable memory (Page 4, paragraph [0052] discloses a proposed extended OTP, one time programmable, memory cell), wherein the improvement comprises an array of transistors (FIG. 4 shows an array of memory cell transistors 402, 404 and the like), wherein at least one of said transistors is programmed using hot carrier transistor aging to alter a characteristic of said at least one of said transistor (FIG. 6, page 3, paragraph [0040] disclose an OTP cell programmed by hot-electron (hot carrier) wherein, a high positive voltage applied to the source or drain accelerates electron carriers through the transistor channel and at the same time a high positive voltage applied to the gate of the transistor pulls the carriers to the transistor thin oxide); and a circuit for sensing said altered characteristic of said at least one of said transistor (**(Note: detecting defined as sensing by a read operation, after programming, of a memory cell in the specifications on page 4, last**

paragraph). FIG. 12, 1200 used for programming or reading, also see page 4, paragraph [0054]).

As to **claim 12**, see rejection to claim 2.

As to **claim 13**, see rejection to claim 3.

As to **claim 14**, see rejection to claim 4.

As to **claim 15**, see rejection to claim 5.

As to **claim 21**, Lee discloses a one time programmable memory element (Page 4, paragraph [0052] discloses a proposed extended OTP, one time programmable, memory cell), wherein the improvement comprises comprising at least one transistor (FIG. 4 shows at least one transistor memory cell 402) that is programmed using hot carrier transistor aging to alter a transistor characteristic (FIG. 6, page 3, paragraph [0040] disclose an OTP cell programmed by hot-electron (hot carrier) wherein, a high positive voltage applied to the source or drain accelerates electron carriers through the transistor channel and at the same time a high positive voltage applied to the gate of the transistor pulls the carriers to the transistor thin oxide); and a circuit for sensing said altered characteristic of said transistor (**(Note: detecting defined as sensing by a read operation, after programming, of a memory cell in the specifications on page 4, last paragraph).** FIG. 12, 1200 used for programming or reading, also see page 4, paragraph [0054]).

As to **claim 23**, see rejection to claim 3.

As to **claim 24**, Lee discloses a memory cell (FIG. 1A, and page 1, paragraph [0006] disclose a one transistor memory cell capable of storing binary data formed in an n-well), comprising only one transistor (FIG 1A transistor memory cell formed in an n-well capable of storing binary data; also see page 1, paragraph [0006]), wherein the improvement of said transistor comprises: a source region (FIG. 1A source region corresponding to either of the P+ doped deposited areas); a drain region (FIG. 1A source region corresponding to either of the P+ doped deposited areas); a channel region (FIG. 1A channel region between the P+ S/D regions and under the gate FG); one silicon-dioxide gate insulator layer (FIG. 1A silicon dioxide above the channel region and below the gate FG; also see page 1, paragraph [0006]); and one gate electrode layer (FIG 1A gate electrode FG).

As to **claim 25**, Lee discloses that the memory cell element is a one time programmable memory element (Page 4, paragraph [0052] discloses a proposed extended OTP, one time programmable, memory cell) programmed using a hot carrier transistor aging technique (FIG. 6, page 3, paragraph [0040] disclose an OTP cell programmed by hot-electron (hot carrier) wherein, a high positive voltage applied to the source or drain accelerates electron carriers through the transistor channel and at the same time a high positive voltage applied to the gate of the transistor pulls the carriers to the transistor thin oxide) to alter a characteristic of said transistor (page 3, paragraph [0042] disclose that after programming, the charge stored is removed and “threshold voltage of memory

cell descends from program cell Vt;" that is, the initial non-programmed cell has achieved a threshold voltage value after programming).

As to **claim 26**, Lee discloses a plurality of said memory cells arranged in an array of rows and columns (FIG. 4 shows a plurality of memory cells 402, 404 arranged in rows and columns).

As to **claim 27**, Lee discloses an integrated circuit (Page 1, paragraph [0001] discloses a non-volatile memory device with CMOS logic process; that is, an integrated circuit (IC) built on a semiconductor CMOS process technology) wherein the improvement comprises comprising: a one time programmable memory (Page 4, paragraph [0052] discloses a proposed extended OTP, one time programmable, memory cell), comprising an array of transistors (FIG. 4 shows a plurality of memory cells 402, 404 arranged in rows and columns), wherein at least one of said transistors is programmed using hot carrier transistor aging (FIG. 6, page 3, paragraph [0040] disclose an OTP cell programmed by hot-electron (hot carrier) wherein, a high positive voltage applied to the source or drain accelerates electron carriers through the transistor channel and at the same time a high positive voltage applied to the gate of the transistor pulls the carriers to the transistor thin oxide) to alter a characteristic of said at least one of said transistor (page 3, paragraph [0042] disclose that after programming, the charge stored is removed and “threshold voltage of memory cell descends from program cell Vt;" that is, the initial non-programmed cell has achieved a threshold voltage value after programming); and a circuit for sensing said altered

characteristic of said at least one of said transistor (**(Note: detecting defined as sensing by a read operation, after programming, of a memory cell in the specifications on page 4, last paragraph).** FIG. 12, 1200 used for programming or reading, also see page 4, paragraph [0054]).

As to **claim 28**, see rejection to claim 2.

As to **claim 29**, see rejection to claim 3.

As to **claim 30**, Lee discloses that said circuit senses said change in said threshold voltage of said at least one of said transistors. (**(Note: detecting defined as sensing by a read operation, after programming, of a memory cell in the specifications on page 4, last paragraph).** Page 3, paragraph [0043] disclose a reading operation for sensing the programmed threshold voltage; that, as disclosed in Table 1, the transistor memory is biased differently from that of programming so as to not to disturb the programming threshold voltage, thus sensing and unchanging the threshold voltage as set by programming; further, FIG. 12 and page 4, paragraph [0054] disclose a unit for reading (sensing) 1200).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claim(s) 6 and 16** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Publication No. 2005/0146932 A1 to Lee et al. ("Lee") in view of U.S. Patent No. 6920067 B2 to Hsu et al. ("Hsu").

As to **claim 6**, Lee discloses said detecting step further comprises the steps of raising a source terminal for each of said array of transistors to a positive potential (FIG. 4 and Page 3, paragraph [0043] discloses the bit line BL0 (source/drain side of memory transistors 402 and 404) is raised to around 1V); raising a gate terminal for all transistors along a selected row to a positive potential (FIG. 4 and page 3, paragraph [0043] discloses applying a voltage VR to the gate terminal of transistors 402 and 404 sharing gate terminal corresponding to VCN).

Lee does not expressly disclose detecting whether a drain voltage changes from a precharge voltage level to approximately a cell transistor threshold voltage below said positive gate terminal potential.

Hsu teaches detecting whether a drain voltage changes from a precharge voltage level to approximately a cell transistor threshold voltage below said positive gate terminal potential (FIG. 6 and Column 4, lines 63-column 5, down to line 8 teach, in a reading operation of a programmed cell, the gate voltage V_{FG} subtracted from the source/drain voltage terminal V_S is smaller than threshold voltage V_{THP} of the transistor (V_{FG}-V_s<V_{THP}), that is, the drain voltage will change by approximately a threshold voltage V_{THP} below V_{FG} (V_S approximately equal to V_{FG}-V_{THP}))

Lee and Hsu are analogous art because they are from the same field of endeavor regarding semiconductor memory circuit design, more specifically OTP memory.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to detecting whether a drain voltage changes from a precharge voltage level to approximately a cell transistor threshold voltage below said positive gate terminal potential as taught by Hsu in the above claim limitation. The suggestion/motivation would have been to apply the teachings offered by Hsu in designing and implementing OTP memory cell programming/reading testing methods at wafer level and IC final test to improve IC production yields based on the concept of threshold voltage expectation.

Therefore, it would have been obvious to combine Lee with Hsu to make the above modification/combination.

As to **claim 16**, see rejection to claim 6.

5. **Claim(s) 7-10, 17-20, 22 and 31** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Publication No. 2005/0146932 A1 to Lee et al. ("Lee") in view of U.S. Patent No. 5751635 to Wong et al. ("Wong").

As to **claim 7**, Lee discloses substantially the claimed invention except that said altered characteristic is a change in a saturation current of said at least one of said transistors.

Wong teaches that said altered characteristic is a change in a saturation current of said at least one of said transistors (FIG. 18b and column 20, lines 39-

43 teach the defining definition of reading a memory cell amounting to measuring (detecting) the programmed threshold voltage; consequently, lines 58-67 teach, with the help of fig. 18b, that as the programmed threshold voltage increases the saturation current decreases. That is the saturation current is altered).

Lee and Wong are analogous art because they are from the same field of endeavor regarding semiconductor memory circuit design, more specifically programming of memory using hot electron (hot carrier).

At the time of invention, it would have been obvious to a person of ordinary skill in the art to determine that said altered characteristic is a change in a saturation current of said at least one of said transistors as taught by Wong in the above claim limitation. The suggestion/motivation would have been to apply the teachings offered by Wong in designing and implementing OTP memory cell programming/reading testing methods at wafer level and IC final test to improve IC production yields based on the concept of threshold voltage expectation.

Therefore, it would have been obvious to combine Lee with Wong to make the above modification/combination.

As to **claim 8**, Lee discloses said programming step further comprising the step of applying a stressful voltage to a source and a gate of said at least one of said transistors (FIG. 6 and page 3, paragraph [0040] disclose applying a high voltage VPP1 to the gate of memory transistor 80 and a high voltage VPP1 to the source of transistor 80).

Wong teaches programming causing said change in said saturation current of said of said at least one of said transistors (FIG. 18b and column 20, lines 39-43 teach the defining definition of reading a memory cell amounting to measuring (detecting) the programmed threshold voltage; consequently, lines 58-67 teach, with the help of fig. 18b, that as the programmed threshold voltage increases the saturation current decreases. That is the saturation current is altered).

For suggestion/motivation, see claim 7.

As to **claim 9**, Lee discloses the step of detecting said programmed at least one of said transistors by sensing said change in said saturation current of said at least one of said transistors (Note: detecting defined as a read operation, after programming, of a memory cell in the specifications. Lee discloses sensing by reading the threshold voltage as follows: page 3, paragraph [0043] disclose a reading operation for sensing the programmed threshold voltage; that is, as disclosed in Table 1, the transistor memory is biased differently from that of programming so as to not to disturb the programming threshold voltage, thus sensing and unchanging the threshold voltage as set by programming).

Lee does not expressly disclose sensing said change in said saturation current.

Wong teaches sensing said change in said saturation current (FIG. 18b and column 20, lines 39-43 teach the defining definition of reading a memory cell amounting to measuring (detecting) the programmed threshold voltage;

consequently, lines 58-67 teach, with the help of fig. 18b, that as the programmed threshold voltage increases the saturation current decreases. That is the saturation current is altered. Further, the relationship between threshold voltage and saturation current is extraordinarily well known in the art and has given rise to very typical, well known and studied I-V curves such as the one of fig. 18b).

For suggestion/motivation, see claim 7.

As to **claim 10**, Lee discloses said detecting step further comprises the steps of raising the voltage on at least one column in said array of transistors to a positive potential (FIG. 4 and Page 3, paragraph [0043] discloses the bit line BL0 (source/drain side of memory transistors 402 and 404) is raised to around 1V); raising a gate terminal of each transistor in a selected row to a positive potential and evaluating a rate of voltage decay of at least one column in said array of transistors (FIG. 4 and page 3, paragraph [0043] discloses applying a voltage VR to the gate terminal of transistors 402 and 404 sharing gate terminal corresponding to VCN).

As to **claim 17**, see rejection to claim 7.

As to **claim 18**, see rejection to claim 8.

As to **claim 19**, see rejection to claim 9.

As to **claim 20**, see rejection to claim 10.

As to **claim 22**, see rejection to claim 7.

As to **claim 31**, see rejection to claim 7.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. U.S. Patent No. 6020227 to Bulucea discloses transistor with threshold adjust doping.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to FERNANDO N. HIDALGO whose telephone number is (571)270-3306. The examiner can normally be reached on Monday-Friday, 7:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Huan Hoang/
Primary Examiner, Art Unit 2827

/Fernando N. Hidalgo/

Examiner, Art Unit 2827